Claims

1. A digital signal delay device for converting a signal (IN) into a corresponding delayed signal (OUT), comprising a plurality of signal delay elements connected in series, wherein, as a function of the desired delay of the delayed signal (OUT), the respective output signal of a particular signal delay element is used for generating the delayed signal (OUT), wherein said signal delay elements each comprise one single inverter only.

2. The digital signal delay device according to claim 1, wherein as a function of the respectively desired delay, the output signal of the respective signal delay element used for generating the delayed signal (OUT) is inverted or non-inverted vis-à-vis the signal (IN).

3. The digital signal delay device according to claim 1, wherein said signal delay device comprising at least three signal delay elements connected in series.

4. The digital signal delay device according to claim 3, wherein said signal delay elements are respectively connected with corresponding gates.

5. The digital signal delay device according to claim 4, wherein as a function of the respectively desired delay – that gate is activated that is connected to the signal delay element whose output signal is to be used for generating the delayed signal (OUT).

6. The digital signal delay device according to claim 5, wherein, depending on whether the output signal of a particular signal delay element is inverted or non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in non-inverted or in inverted manner.

7. The digital signal delay device according to claim 6, wherein when the output signal of a particular signal delay element is inverted vis-à-vis the signal (IN), the gate

connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner.

8. The digital signal delay device according to claim 6, wherein when the output signal of a particular signal delay element is inverted vis-à-vis the signal (IN), the gates connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner.

9. The digital signal delay device according to claim 8, wherein the gate, depending on whether they are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN) – comprise an inverter circuit arrangement or a transfer gate circuit arrangement.

10. The digital signal delay device according to claim 8, wherein the gates, depending on whether they are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN) – comprise two inverter circuit arrangements, or a transfer gate circuit arrangement and an inverter circuit arrangement.

11. The digital signal delay device according to claim 8, wherein the gates, depending on whether they are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN) – comprise two inverter circuit arrangements and a transfer gate circuit arrangement, or three inverter circuit arrangements.

12. The digital signal delay device according to claim 11, wherein at least one of the inverter circuit arrangements is a tristate inverter circuit arrangement.

13. The digital signal delay device according to claim 2, wherein said signal delay device comprising at least three signal delay elements connected in series.

14. The digital signal delay device according to claim 13, wherein said signal delay elements are respectively connected with corresponding gates; wherein as a function of the respectively desired delay – that gate is activated that is connected to the signal delay element whose output signal is to be used for generating the delayed signal (OUT); and wherein, depending on whether the output signal of a particular signal delay element is inverted or non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in non-inverted or in inverted manner.

15. The digital signal delay device according to claim 14, wherein when the output signal of a particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner.

16. The digital signal delay device according to claim 14, wherein when the output signal of a particular signal delay element is inverted vis-à-vis the signal (IN), the gates connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner.

17. The digital signal delay device according to claim 16, wherein the gate, depending on whether they are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN) – comprise an inverter circuit arrangement or a transfer gate circuit arrangement.

18. The digital signal delay device according to claim 16, wherein the gates, depending on whether they are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN) – comprise two inverter circuit arrangements, or a transfer gate circuit arrangement and an inverter circuit arrangement.

19. The digital signal delay device according to claim 16, wherein the gates, depending on whether they are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN) – comprise two inverter circuit arrangements and a transfer gate circuit arrangement, or three inverter circuit arrangements.

20. The digital signal delay device according to claim 19, wherein at least one of the inverter circuit arrangements is a tristate inverter circuit arrangement.